REMARKS/ARGUMENTS

Claims 1, 2, 4-8, 10, 11, 13, 14, 16, 18, and 19-23 are pending. Claims 1, 5, 6, 10, 11, and 14 are amended. Claims 3, 9, 12, 15, 17, and 19 are canceled. Claims 21-23 are new. Support for the new and amended claims can be found in the specification as originally filed on page 9, ll. 1-26. No new matter is added. Reconsideration and allowance of the claims is requested.

Applicants do not concede that the originally filed claims are not patentable over the art cited by the Examiner, as the present claim amendments and cancellations are included only to facilitate expeditious prosecution. Applicants respectfully reserve the right to pursue these and other claims in one or more continuations and/or divisional patent applications.

I. Claim Objections

The examiner objected to claim 5 on the basis of the recited informality. Applicants amended claim 5 accordingly, thereby overcoming the objection.

II. 35 U.S.C. § 101: Asserted Non-Statutory Subject Matter

The examiner rejected claims 10-14, 19, and 20 under 35 U.S.C. § 101 as being directed towards non-statutory subject matter. Applicants have amended these claims accordingly to overcome the rejection.

III. 35 U.S.C. § 102: Asserted Anticipation

The examiner rejects claims 6-13 and 17-20 under 35 U.S.C. § 102 as anticipated by *Baxter et al.*, High Availability Computer system and Methods Related Thereto, U.S. Patent 6,122,756 (September 19, 2000) (hereinafter "*Baxter*"). This rejection is respectfully traversed. In rejecting claim 6, the examiner states that:

> 5. Referring to claim 6, Baxter discloses a computer system, having at least one processor, memory, and a bus coupled between the memory and the processor, comprising: a plurality of hardware units connected to the computer system by the bus (See figures 2-12);
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> a service processor having firmware (From line 1 of column 22, "As provided above, the EEPROMS 302 include the firmware for the microcontroller 300 and the JPs 250, particularly the JP designated as the diagnostic master and the microcontroller designated as the master microcontroller. The firmware for the microcontroller includes powerup testing, scan testing, error handling, system sniffing during run-time, and scanning error state when system fatal error occurs. The JP firmware includes powerup tests, XDIAG tests, manufacturing mode tests, and error handling.");

> wherein when a first hardware unit of the plurality experiences an error, the first hardware unit is disconnected from the bus; and wherein the computer system is restarted without running a first diagnostic associated with the first hardware unit (From line 28 of column 16, "Such scanning is done when the system is powered up and also after the system detects a fatal error. The scanning operation includes automatically detecting a fault, automatically isolating the fault to at least a FRU and automatically deconfiguring the system so as to logically and functionally removed the isolated component/FRU. After the system is deconfigured, the system automatically re-boots itself and re-loads any applications program." From line 36 of column 24, "The master microcontroller runs the remaining off-board scan tests including power supply, blower, and backpanel interconnect testing. Any motherboards that were deconfigured as a result of previous testing will not be included in backpanel interconnect testing." Further, logically, if it is thusly disconnected it could not be tested.).

Office action of September 25, 2007, pp. 3-4.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case, each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Claim 6 as amended is as follows:

> 6. (Currently Amended) A computer system, having at least one processor, memory, and a bus coupled between the memory and the processor, comprising:
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> a plurality of hardware units connected to the computer system by the bus;
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> a service processor having firmware;
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> wherein when a first hardware unit of the plurality experiences an error, the first hardware unit is disconnected from the bus, wherein the error comprises a common bus interface error, and wherein a set of additional functional units associated with the common bus interface error are also disconnected from the bus; and
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> wherein the computer system is restarted without running a first diagnostic associated with the first hardware unit and the set of functional units.

Claim 6 as amended contains the newly added features of, "wherein a set of additional functional units associated with the common bus interface error are also disconnected from the bus," and "wherein the computer system is restarted without running a first diagnostic associated with the first hardware unit and the set of functional units." *Baxter* does not teach these claimed features.

Baxter teaches a high availability computer system. *Baxter*, Abstract. Specifically, *Baxter* teaches that motherboards of a multi-motherboard system can be deconfigured and thus excluded from operation of the overall data processing system. *Baxter*, Abstract. However, *Baxter* does not teach that a set of additional functional units are associated with a common bus interface error and are also disconnected from the bus, as recited in claim 1. Although the examiner attempts to point out that *Baxter* addresses bus interface errors, *Baxter* still does not teach associating sets of additional functional units with the common bus interface error. Thus, *Baxter* does not teach all of the features of claim 1. Accordingly, under the standards of *In re Bond*, *Baxter* does not anticipate claim 1.

Applicants also note that, contrary to the examiner's assertions, *Baxter* does teach restarting hardware *with* running a diagnostic on the deconfigured hardware. For example, *Baxter* col. 26, ll. 6-27 provides that information regarding failed motherboards is stored in NOVRAM. This information is diagnosed after reboot. *Baxter*, col. 28, l. 65 through col. 29, l. 7. Thus, again, *Baxter* does not teach all of the features of claim 6.

The remaining claims cited in this rejection all contain features similar to those presented in claim 6. Therefore, at least for the reasons given above, this rejection is overcome.

IV. 35 U.S.C. § 103: Asserted Obviousness

The examiner rejected claims 1, 2, 4, 5, 14, 15, and 16 under 35 U.S.C. § 103 as obvious over *Baxter* in view of *Beaujard, et al.*, Process and Device for Identifying Faults in a Complex System, U.S. Patent 5,774,645 (June 30, 1998) (hereinafter "*Beaujard*"). This rejection is respectfully traversed. Applicants note that the rejection of claim 14 is maintained separately; however, the references are the same. In rejecting claim 1, the examiner states that:

> 15. Referring to claim 1, Baxter discloses a method of processing errors in a computer system, having at least one processor, memory, and a bus coupled between the memory and the processor (See figures 2-12), comprising:
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> identifying, by a service processor (From line 23 of column 4, ""Diagnostic Master JP (OM)" shall be understood to mean the job processor/central processing unit in the system that coordinates all inter-board testing and in control when the system first halts into the main user interface."), failed hardware of the computer system (From line 24 of column 16, "The computer system 200 of the instant invention scans the boards, board mounted chips, busses, blowers and power supplies comprising the system to verify the integrity and operability of the system before applications are loaded.");
>
> identifying, by the service processor, other hardware failed hardware within the computer system; deconfiguring the failed hardware and the other failed (From line 18 of column 26, "During the entire process of selecting a diagnostic master all failing tests and resulting motherboard/daughter board deconfigurations will be logged in each boards NOVRAM error log and the NOVRAM configuration

tables. Just as had been done for the on-board microcontroller diagnostics and scan failures. At the completion of selecting the "diagnostic master", the diagnostic master JP will poll the various NOVRAMs to determine complete error and deconfiguration information, if any. All current system configuration information is now be written to the system 10 SEEPROM 204."); and

rebooting the computer system without running a diagnostic on the failed Page 9 hardware (From line 28 of column 16, "Such scanning is done when the system is powered up and also after the system detects a fatal error The scanning operation includes automatically detecting a fault, automatically isolating the fault to at least a FRU and automatically de-configuring the system so as to logically and functionally removed the isolated componentiFRU. After the system is deconfigured, the system automatically re-b09ts itself and re-loads any applications program." From line 36 of column 24, "The master microcontroller runs the remaining off-board scan tests including power supply, blower, and backpanelinterconnect testing. Any motherboards that were deconfigured as a result of previous testing will not be included in backpanel interconnect testing." Further, logically, if it is thusly disconnected it could not be tested.).

Although Baxter does not specifically disclose that this other failed hardware is specifically identified as affected by the failed hardware, identifying such hardware is well known in the art. An example of this is shown by such concepts as root cause analysis, sympathetic errors, hierarchical analysis, etc... However, one specific example is shown by Beaujard, from line 50 of column 2, "Additionally, by grouping together cues, carried out when searching for a faulty element, the cues resulting directly or indirectly from a specified fault are ascertained, which cues need not therefore be taken into account during maintenance." A person of ordinary skill in the art at the time of the invention could have been motivated to identify such related failure because, as shown in Beaujard, it saves time in maintenance, and further, Baxter has shown that such related errors are known, even if they are not explicitly indicated, and that while Baxter isolates as finely as it can, this may not be fine enough, from line 63 of column 6, "The . computer system preferably operates so fault isolation is at least to the FRU which failed or to the FRU on which the component believed to be faulted is located."

Office action of September 25, 2007, pp. 8-10.

The Examiner bears the burden of establishing a *prima facie* case of obviousness based on prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992). The prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka,* 490 F.2d 981, 180 USPQ 580 (CCPA 1974). In determining obviousness, the scope and content of the prior art are... determined; differences between the prior art and the claims at issue are... ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background the obviousness or non-obviousness of the subject matter is determined. *Graham v. John Deere Co.*, 383 U.S. 1 (1966). "Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace;

and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR Int'l. Co. v. Teleflex, Inc.*, No. 04-1350 (U.S. Apr. 30, 2007). "*Rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.* Id. (citing *In re Kahn*, 441 F.3d 977, 988 (CA Fed. 2006))."

Claim 1 as amended is as follows:

> 1. (Currently Amended) A method of processing errors in a computer system, having at least one processor, memory, and a bus coupled between the memory and the processor, comprising:
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> identifying, by a service processor, failed hardware of the computer system;
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> identifying, by the service processor, other hardware affected by the failed hardware within the computer system, wherein the other hardware comprises all functional units associated with a common bus interface error;
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> deconfiguring the failed hardware and the other hardware affected by the failed hardware; and
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> rebooting the computer system without running a diagnostic on the failed hardware.

As noted above, *Baxter* does not teach the claimed features of "wherein the other hardware comprises all functional units associated with a common bus interface error," and "rebooting the computer system without running a diagnostic on the failed hardware." Given the lack of disclosure in *Baxter*, this reference also does not suggest these claimed features.

Additionally, *Beaujard* does not teach or suggest these claimed features. *Beaujard* is directed to the diagnosis and locating of faults in complex computer systems. *Beaujard*, Abstract. Specifically, *Beaujard* divides a complex system into components and then analyzes the components. *Beaujard*, col. 2, ll. 5-11.

However, *Beaujard* is completely devoid of disclosure regarding the claimed feature of, "wherein the other hardware comprises all functional units associated with a common bus interface error." *Beaujard* is also silent with regard to the claimed feature of, "rebooting the computer system without running a diagnostic on the failed hardware." Given the lack of disclosure with regard to these claim features, *Beaujard* also does not suggest these claim features

Because neither references teaches or suggests all of the features of claim 1, the proposed combination of references, considered as a whole, also fails to teach or suggest these claim features. Accordingly, no *prima facie* obviousness rejection can be stated against claim 1 using these references.

The remaining claims in this rejection all contain the features recited in claim 1. Accordingly, at least for the reasons given above, this rejection is overcome.

Additionally, Applicants note that the examiner did not state a proper reason to achieve the *legal conclusion* of obviousness. Instead, the examiner only cited a purported advantage to combining the references without connecting the purported advantage to the legal conclusion of obviousness. Therefore, the obviousness rejection does not comport with the standards of *KSR Int'l.* Hence, in any case, the examiner failed to state a *prima facie* obviousness rejection against the claims.

V. New Claims

New claims 21-23 contain the feature of, "persistently deconfiguring an I/O hub adapter." Neither *Baxter* nor *Beaujard* teach or suggest this claim feature. Accordingly, neither reference, alone or in combination with each other or the other references, renders these claims unpatentable under either 35 U.S.C. § 102 or 35 U.S.C. § 103. Accordingly, these claims should be in condition for allowance.

VI. Conclusion

The subject application is patentable over the cited references and should now be in condition for allowance. The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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